at lease one memory cell of a memory array, that generates a first voltage output and a second voltage output, wherein the first voltage output ramps from a predetermined voltage level to a higher voltage level when the memory cell is accessed, and the second voltage output keeps in a predetermined voltage level;

a first N-type device coupled between ground and one corresponding bit line of the memory array, wherein discharging the bit line voltage when memory array accessing is completed;

a second N-type device coupled between ground and one corresponding bit line-bar of the memory array, wherein discharging the bit line voltage when memory array accessing is completed; and

a differential amplifier with two input nodes coupled to the bit line and the bit line-bar of the memory array to generate a first sense output voltage if the first voltage output of one memory cell is higher than a second voltage output of the one memory cell and to generate a second sense output voltage if the first voltage output of one memory cell is lower than a second voltage output of the one memory cell.

Claim 8. (Amended)

A control circuit for a semiconductor memory array, comprising:

a sense amplifier for amplifying output from a memory cell;

a self-timer coupled to the sense amplifier for counting a first time and sending out control signals to shut off the sense amplifier